**1. Instruction fetch step**

**1.** 指令获取步骤 **state == 0**

IR <= Memory[PC];

PC <= PC + 4;

**2. Instruction decode and register fetch step**

**2.** 指令解码和寄存器获取步骤 **state == 1**

A <= Reg[IR[19:15]];

B <= Reg[IR[24:20]];

ALUOut <= PC + immediate;

**3. Execution, memory address computation, or branch completion**

**3.** 执行、内存地址计算或分支完成 **state == 2**

Memory reference:内存引用：immediate

Arithmetic-logical instruction (R-type):算术逻辑指令（R型）：ALUOut <= A op B;

Branch:分支：if (A == B) PC <= ALUOut;

**4. Memory access or R-type instruction completion step**

**4.** 内存访问或**R**型指令完成步骤 **state == 3**

Memory reference:内存引用：

MDR <= Memory [ALUOut]; or或者 Memory [ALUOut] <= B;

Arithmetic-logical instruction (R-type):算术逻辑指令（R型）:

Reg[IR[11:7]] <= ALUOut;

**5. Memory read completion step**

**5.** 内存读取完成步骤 **state == 4**

Load:载入：Reg[IR[11:7]] <= MDR;